WHAT IS CLAIMED IS:

1. A method of providing first and second output signals in response to first and second input signals, comprising:

providing the first and second input signals at complementary logic states;

providing first and second intermediate signals on first and second nodes at the complementary logics states in response to the providing the first and second input signals at the complementary logic states;

providing a first clocked inverter having a signal input coupled to the first node, a signal output coupled to the second node, and a clock input;

providing a second clocked inverter having a signal input coupled to the second node, a signal output coupled to the first node, and a clock input;

providing the first and second input signals at a predetermined one of the complementary logic states after providing the first and second input signals at the complementary logic states;

enabling the clock inputs of the first and second clocked inverters prior to providing the first and second input signals at the predetermined one of the complementary logic states whereby the first and second intermediate signals at the complementary logic states are latched; and

providing the first and second output signals responsive to the first and second intermediate signals.

2. The method of claim 1, wherein the first and second clocked inverters have second clock inputs, further comprising enabling said second clock inputs in response to providing the first and second input signals at the complementary logic states.

3. The method of claim 1, wherein the first and second clocked inverters are characterized as inverting only one of the complementary logic states when the clock inputs are disabled and inverting both complementary logic states when the clock inputs are enabled.

4. The method of claim 1, wherein providing the first and second intermediate signals is achieved by third and fourth clocked inverters responsive to the first and second input signals.

5. The method of claim 4, wherein the third and fourth clocked inverters are characterized as inverting only one of the complementary logic states when the clock inputs are disabled and inverting both complementary logic states when the clock inputs are enabled.

6. A method of providing first and second output signals in response to first and second input signals, comprising:

providing the first and second input signals at complementary logic states;

providing first and second intermediate signals on first and second nodes at the complementary logics states in response to the providing the first and second input signals at the complementary logic states;

providing a first clocked inverter having a signal input coupled to the first node, a signal output coupled to the second node, and a clock input;

providing a second clocked inverter having a signal input coupled to the second node, a signal output coupled to the first node, and a clock input;

providing the first and second input signals at a predetermined one of the complementary logic states during a precharge phase;

enabling the clock inputs of the first and second clocked inverters in response to entering the precharge phase; and

providing the first and second output signals responsive to the first and second intermediate signals.

7. The method of claim 6, wherein the first and second inverters have second clock inputs, further comprising enabling said second clock inputs in response to providing the first and second input signals at the complementary logic states.

8. The method of claim 6, wherein providing the first and second intermediate signals is achieved by third and fourth clocked inverters responsive to the first and second input signals.

9. The method of claim 8, wherein the third and fourth clocked inverters are characterized as inverting only one of the complementary logic states when the clock inputs are disabled and inverting both logic states when the clock inputs are enabled.

10. A circuit, comprising:

a first clocked inverter having a signal input for receiving a first input signal, a clock input responsive to a clock signal, and an output;

a second clocked inverter having a signal input for receiving a second input signal, a clock input responsive to the clock signal, and an output;

a third clocked inverter having a signal input coupled to the output of the first clocked inverter, a clock input responsive to the clock signal, and an output;

a fourth clocked inverter having a signal input coupled to the output of the second clocked inverter, a clock input responsive to the clock signal, and an output, wherein the output of the fourth clocked inverter is coupled to the input of the third clocked inverter and the output of the third clocked inverter is coupled to the input of the fourth clocked inverter.

11. The circuit of claim 10 further comprising:

a first inverter having an input coupled to the output of the first clocked inverter and an output for providing a first output signal; and

a second inverter having an input coupled to the output of the second clocked inverter and an output for providing a second output signal.

12. The circuit of claim 10, wherein the first clocked inverter comprises:

a first transistor having a control electrode coupled for receiving the first input signal, a first current electrode coupled to a first power supply terminal, and a second current electrode;

a second transistor having a control electrode coupled for receiving the first input signal, a first current electrode coupled to the second current electrode of the first transistor, and a second current electrode; and

a third transistor having a control electrode coupled to be responsive to the clock signal, a first current electrode coupled to the second current electrode of the

second transistor, and a second current electrode coupled to a second power supply terminal.

13. The circuit of claim 12, wherein the third clocked inverter comprises:

a fourth transistor having a control electrode coupled to the second current electrode of the first transistor, a first current electrode coupled to the second power supply terminal, and a second current electrode coupled to the output of the second clocked inverter;

a fifth transistor having a control electrode coupled to the second current electrode of the first transistor, a first current electrode coupled to the second current electrode of the fourth transistor, and a second current electrode; and

a sixth transistor having a control electrode coupled to be responsive to the clock signal, a first current electrode coupled to the second current electrode of the fifth transistor, and a second current electrode coupled to the first power supply terminal.

14. The circuit of claim 13, wherein the third and fourth transistors are P channel transistors.

15. The circuit of claim 10, wherein the first clocked inverter comprises:

a first transistor having a control input for receiving the first signal, a first current electrode coupled to a first power supply terminal, and a second current electrode coupled to the signal input of the third clocked inverter;

a second transistor having a control input for receiving the clock signal, a first current electrode coupled to the second current electrode of the first transistor, and a second current electrode; and

a third transistor having a control electrode for receiving a control signal, a first current electrode coupled to the second current electrode of the second transistor, and a second current electrode coupled to a second power supply terminal.

16. A circuit, comprising:

a first inverting circuit having a signal input for receiving a first input signal and an output;

a second inverting circuit having a signal input for receiving a second input signal and an output;

a first clocked inverter having a signal input coupled to the output of the first inverting circuit, a clock input responsive to a clock signal, and an output; and

a second clocked inverter having a signal input coupled to the output of the second inverting circuit, a clock input responsive to the clock signal, and an output;

17. The circuit of claim 16, wherein the first clocked inverter comprises:.

a first transistor having a control electrode coupled to the output of the first inverting circuit, a first current electrode coupled to a first power supply terminal, and a second current electrode;

a second transistor having a control electrode coupled to the output of the first inverting circuit, a first current electrode coupled to the second current electrode of the first transistor, and a second current electrode; and

a third transistor having a control electrode coupled to be responsive to the clock signal, a first current electrode coupled to the second current electrode of the second transistor, and a second current electrode coupled to a second power supply terminal.

18. The circuit of claim 16, wherein the first inverting circuit is further characterized as having a clock input and wherein the first inverting circuit comprises:

a first transistor having a control electrode coupled for receiving the first input signal, a first current electrode coupled to a first power supply terminal, and a second current electrode;

a second transistor having a control electrode coupled for receiving the first input signal, a first current electrode coupled to the second current electrode of the first transistor, and a second current electrode; and

a third transistor having a control electrode coupled to be responsive to the clock signal, a first current electrode coupled to the second current electrode of the

second transistor, and a second current electrode coupled to a second power supply terminal.

19. The circuit of claim 16, wherein the first inverting circuit is further characterized as having a clock input and wherein the first inverting circuit comprises:

a first transistor having a control electrode for receiving the first signal, a first current electrode coupled to a first power supply terminal, and a second current electrode coupled to the signal input of the first clocked inverter;

a second transistor having a control input for receiving the clock signal, a first current electrode coupled to the second current electrode of the first transistor, and a second current electrode; and

a third transistor having a control electrode for receiving a control signal, a first current electrode coupled to the second current electrode of the second transistor, and a second current electrode coupled to a second power supply terminal.

20. The circuit of claim 19, further comprising:

a first inverter having an input for receiving a first primary input signal and an output for providing the first input signal;

a second inverter having an input for receiving a second primary input signal and an output for providing the second input signal; and

a logic gate having a first input for receiving the first primary input signal, a second input for receiving the second input signal, and an output for providing the control signal.

21. The circuit of claim 16, further comprising:

a first inverter having an input coupled to the output of the first clocked inverter and an output for providing a first output signal; and

a second inverter having an input coupled to the output of the second clocked inverter and an output for providing a second output signal.

22. A circuit comprising a domino-compatible latch, the latch comprising:
complementary input inverters;
input control circuitry coupled to the input inverters to selectively configure the input inverters to prevent an output of each input inverter from making a first signal transition type;
cross-coupled storage inverters, each storage inverter having an input coupled to receive a signal from an output of one of the input inverters; and
storage control circuitry coupled to selectively configure the storage inverters to prevent an output of each storage inverter from making a second signal transition type.

23. The circuit of 22 wherein the first transition type is a transition from low to high.

24. The circuit of 22 wherein the second transition type is a transition from high to low.

25. The circuit of 22 wherein the first transition type is a transition from a first signal level corresponding to a first power rail value to a second signal level corresponding to a second power rail value and the second transition type is a transition from the second signal level to the first signal level.

26. A latch comprising:
a clocked input stage coupled to receive first and second complementary input signals;
a clocked storage stage coupled to the clocked input stage, the clocked storage stage comprising two cross-coupled inverters, wherein each of the invertors are clocked.
an output stage coupled to the clocked storage stage to provide first and second complementary output signals.